CLAIMS

What is claimed is:

1. A method for manufacturing a semiconductor integrated circuit, the method comprising:

providing a wafer having a plurality of integrated circuit dies;

using a test fixture to provide electrical contact with electrical testing structures located in a scribe line adjacent to a first of the plurality of integrated circuit dies; and

monitoring the output of an identification cell located within the first of the plurality of integrated circuit dies by using the test fixture to provide contact with contacts on the wafer corresponding to the identification cell.

2. The method as recited in claim 1 wherein the contacts are electrically connected to the identification cell and positioned in a predetermined standardized geometric location relative to the electrical testing structures located in the scribe line.

3. The method as recited in claim 1 wherein the contacts are metallic pads.

4. The method as recited in claim 1 further comprising using the test fixture to access a contact on at least one of the plurality of integrated circuit dies to measure a performance parameter.

5. The method as recited in claim 4 wherein the performance parameter is one of a supply current and a supply voltage.

6. The method as recited in claim 4 wherein the performance parameter is a quiescent current.

7. The method as recited in claim 1, wherein the output of an identification cell provides a unique identification number for the cell and further comprising storing the identification number along with location data indicating the location of the first of the plurality of integrated circuit dies on the wafer.

8. The method as recited in claim 7 further comprising using the identification number and the location data in a post processing step to identify defects in the plurality of dies.

9. An integrated circuit test fixture configured for interconnection between a semiconductor tester and a wafer, comprising:

a plurality of probe tips configured to provide electrical contact with a corresponding plurality of pads on a semiconductor wafer, wherein a first group of the plurality of pads comprises pads connected to an identification cell located within an integrated circuit die on the wafer and a second group of the plurality of pads is connected to an electrical testing structure located in a scribe line adjacent to the die.

10. The integrated circuit test fixture as recited in claim 9 wherein the plurality of pads are located in a corner of the integrated circuit die adjacent to the location of electrical testing structure located in a scribe line adjacent to the die.

11. The integrated circuit test fixture as recited in claim 9 wherein a third group of the plurality of pads is connected to a reference test cell located on the integrated circuit die and configured to measure an electrical parameter for the integrated circuit.

12. The integrated circuit test fixture as recited in claim 11 wherein the electrical parameter is a supply current.

13. The integrated circuit test fixture as recited in claim 9 wherein the plurality of probe tips are connected to a printed circuit board of the test fixture, the printed circuit board configured for electrical connection to a tester.

14. A method of manufacturing a semiconductor integrated circuit, the method comprising:

providing a wafer having a plurality of dies;

generating an identification number from an identification cell located on each of the plurality of dies;

monitoring the identification number before separating the plurality of dies from the wafer by using a generic interface configured to access pads on a plurality of different integrated circuit designs; and

using the monitored identification number in a statistical post processing to identify defects in any of the plurality of dies.

15. The method recited in claim 14, wherein the statistical post processing identifies wafer defect patterns.

16. The method recited in claim 15, further comprising correlating the monitoring identification number with a physical location of the die on the wafer and wherein the wafer defect patterns are determined using the identification number and the physical location of the die on the wafer.

17. The method recited in claim 15, wherein the generic interface is configured to conform to a standardized configuration of pads on the wafers.

18. The method recited in claim 15, wherein the test interface is configured to access e-test structure pads at the same time that the identification cell signals are monitored.

19. The method recited in claim 18, further comprising monitoring a signal from a reference test cell within at least one of the plurality of dies.

20. The method recited in claim 14 wherein the post processing occurs after the plurality of dies are separated from the wafer.